AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0005] on page 1, lines 12 to 13 as follows:

[0005] Therefore, a logic emulation device that reproduces (emulates) circuit operation by hardware ~~are~~ is used.

Please amend paragraph [0022] on page 2, line 27 to page 3, line 2 as follows:

[0022] The technique of allotting a logic circuit to an FPGA in a unit of cluster has a purpose to avoid ~~the~~ a lack in ~~the~~ a number of I/O (input/output) of the FPGA, which is indicated by Rent's rule.

Please amend paragraph [0029] on page 3, lines 15 to 16 as follows:

[0029] Process with thinner lines of today's semiconductors has made LSIs even ~~much~~ more larger-scaled, which has made it more difficult to allot logic circuits to FPGAs.

Please amend paragraph [0101] on page 10, lines 22 to 24 as follows:

[0101] Fig. 2 is a block diagram illustrating the circuit allocation device 1 in Fig. 1. Additionally, components same as or similar to those of Fig. 2 are ~~attached~~ identified with the same reference symbols or numerals of those of Fig. 1.

Please amend paragraph [0121] on page 12, lines 23 to 25 as follows:

[0121] The circuit dividing unit 85 inserts a dividing flip-flop FF2 into the cluster C, and the clustering unit 80 practices re-clustering for the cluster C ~~that~~ into which the dividing the flip-flop FF2 has been inserted.

Please amend paragraph [0131] on page 14, lines 5 to 6 as follows:

[0131] As described above, the clustering unit 80 practiced re-clustering for the cluster C ~~that~~ into which the dividing flip-flop FF2 had been inserted, and created the clusters C1 and C2.

Please amend paragraph [0155] on page 16, lines 20 to 22 as follows:

[0155] Fig. 6 shows an example ~~that~~ in which the operation clock FCLK of the dividing flip-flop inserted in the cluster in Fig. 5 is a pulse-shaped clock that synchronizes with the falling edge of the operation clock CLK of the flip-flops FF0-FF4.

Please amend paragraph [0203] on page 21, lines 16 to 21 as follows:

[0203] Then the optimized-logic-circuit-information generating unit 88 practices an allotting process again for the plurality of clusters obtained by subdividing the cluster 22, and updates the optimized logic circuit information 11. The practice of the allotting process is carried out under the condition of the circuit scale (the number of circuits (gates)) that can be allotted in the vacant area of the FPGA20 and the number of I/Os of the ~~FPGA20;~~ FPGA20.

Please amend paragraph [0205] on page 21, lines 24 to 25 as follows:

[0205] Except for the above description, the second embodiment is the same as the first embodiment, thereby, further explanation is omitted.

Please amend paragraph [0299] on page 31, lines 7 to 10 as follows:

[0299] At step S0, referring to the memory substitution table information, the substituting unit 95 ~~substitute~~ substitutes a logic circuit for a memory device to be logically emulated, by expressing a memory device that realizes the memory device to be logically emulated, in terms of circuit length,.